REMARKS

The Applicant would like to thank Examiner Joni Hsu for extending the courtesy of a teleconference on June 23, 2009. During the call, the Examiner and the Applicant discussed several aspects of the claimed invention which were not disclosed by the combined Levy device. The following remarks and comments memorialize the conversation, and the Applicant kindly requests the Examiner to reconsider the rejection in view of the following:

Claim 1 as amended requires:

1. A motherboard, comprising:

a chipset for managing data transfers within the motherboard;

a scalable interconnect connecting to the motherboard, said scalable interconnect supporting a number of interconnect lanes;

plurality of high-speed video card slots connected to the interconnect, the high speed video card slots including at least one first video card slot and second video card slot; and

a switch connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots,

wherein the motherboard enables a first and a second video card to attach, respectively, to the at least one first video card slot and second video card slot, wherein the motherboard enables the first and the second video cards to operate in parallel to output graphics data to a single visual display device, and wherein said switch is configured to distribute lanes dynamically during operation to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards.

REMARKS

I) PORT TRANSMITTER 116 OF LEVY DOES NOT DISCLOSE A SWITCH CAPABLE OF CONVERTING THE INTERCONNECT LANES INTO A PLURALITY OF DISTRIBUTED LINKS SUCH THAT THERE IS A DIFFERENT ONE OF SAID DISTRIBUTED LINKS PROVIDING A CONNECTION EACH OF SAID PLURALITY OF HIGH-SPEED VIDEO CARDS SLOTS

The Examiner has argued (on page 3, column 4 of the 3/34/09 Office action) that Levy's port transmitter is equivalent to a switch "capable of converting the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection each of said plurality of high-speed video cards slots" because, Levy describes:

> [0075] In general, system designer to route signal lines between ports with minimal limitations imposed by the location of the device ports. In general, the system designer may simply interconnect ports in a manner that eases physical routing and allow the port identification methods of the devices discover/identify the port connections. Further, the port identification methods provide the system designer with fine grain control of bandwidth between devices by allowing the system designer to assign lanes to links on a per lane basis.

Despite paragraph's [0075] disclosure, Levy does not disclose ***the port transmitter 116*** has this functionality, rather Levy broadly attributes this functionality to the system (hence the underlined text above). Levy's disclosure of the port transmitted is confined to three paragraphs. Levy discloses:

> [0021] Referring now to FIG. 3, an embodiment of a root interface (e.g. DEVICE 0 interface) is depicted. The root interface may comprise one or more ports 112.sub.1 . . . 112.sub.X. The ports 112.sub.1 . . . 112.sub.X may comprise port receivers 114.sub.1 . . . 114.sub.X and port transmitters 116.sub.1 . . . 116.sub.X. In one embodiment, each port receiver 114.sub.1 . . . . 114.sub.X receives low voltage differential signals that are serially provided on a pair of receive lines, and each port transmitter 116.sub.1 . . . 116.sub.X serially transmits low voltage differential signals on a pair of transmit lines. However, in other embodiments, the port receivers 114.sub.1 . . . 114.sub.X and corresponding port transmitters 116.sub.1 . . . 116.sub.X may be implemented using other signaling technologies such as, for example, optical, synchronous, source synchronous, asynchronous, etc. In another embodiment, the ports 112.sub.1 . . . 112.sub.X may comprise port transceivers having a unified transmitter/receiver instead of separate port receivers 114.sub.1 . . . 114.sub.X and port transmitters 116.sub.1 . . . 116.sub.X

as depicted.

[0022] The ports 112.sub.1 . . . 112.sub.X may further comprise one or more decoders 181.sub.1 . . . 118.sub.X to decode encoded data units or symbols received from its corresponding port receiver 114.sub.1 . . . 114.sub.X, and may also comprise one or more encoders 120.sub.1 . . . 120.sub.X to generate encoded data units or symbols to be transmitted by its corresponding port transmitter 116.sub.1 . . . 116.sub.X. In another embodiment, the ports 112.sub.1 . . . 112.sub.X may comprise one or more codecs that comprise a unified encoder/decoder instead of separate decoders 118.sub.1 . . . 118.sub.X and encoders 120.sub.1 . . . 120.sub.X as depicted. Further, the decoders 118.sub.1 . . . 118.sub.X and the encoders 120.sub.1 . . . 120.sub.X may comprise buffers to provide buffer storage for data units and symbols being transferred.

[0023] The decoders 118.sub.1 . . . 118.sub.X and encoders 120.sub.1 . . . 120.sub.X may implement the well known 8b/10b encoding scheme which is described in PCI Express Base Specification, Revision 1.0, Jul. 22, 2002 and may respectively implement scramblers and descramblers. Generally, in such an encoding scheme, the decoders 118.sub.1 . . . 118.sub.X decode 10 bit symbols received from the port receivers 114.sub.1 . . . 114.sub.X to obtain 8 bit data units, and the encoders 120.sub.1 . . . 120.sub.X encode 8 bit data units to obtain 10 bit symbols to be serially transmitted by the port transmitters 116.sub.1 . . . 116.sub.X. Further, the encoders 120.sub.1 . . . . 120.sub.X may scramble the 10 bit symbols to effectively spread the transfer across a frequency spectrum to reduce generated interference, and the decoders 118.sub.1 . . . 118.sub.X may descramble the transmitted data units to obtain the 10 bit data symbols. Other embodiments of the root device may use a different encoding/decoding scheme or may transfer data units without encoding and/or scrambling. One advantage of the 8b/10b encoding scheme is that a clock signal is effectively embedded in the symbol transmission, thus allowing symbols to be transferred without one or more separate clock signal lines between the transmitter and receiver of the symbols.

Nowhere in this disclosure is any recitation that the ***port transmitter*** can "convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots." In contrast as disclosed in the instant application in paragraphs [0024], [0060] and [0061], the switch of the present invention itself has the ability to "convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots," and therefore Levy does not disclose all the features of Claim 1. The Examiner's reliance on Stufflebeam or Grimaud does not remedy this missing feature of Levy. Claim 41 is allowable for similar reasons.

II) PORT TRANSMITTER 116 OF LEVY DOES NOT DISCLOSE A SWITCH CONFIGURED TO DISTRIBUTE LANES DYNAMICALLY DURING OPERATION TO SAID PLURALITY OF HIGH-SPEED VIDEO CARD SLOTS RESPONSIVE TO CHANGES IN BANDWIDTH NEEDS DURING PROCESSING BY SAID VIDEO CARD

In the claimed invention, the switch can dynamically distribute lanes during the operation of the high speed video cards. *See* paragraphs [0024], [0060] and [0061] of the instant application for example. Levy teaches away from this functionality. Levy's system requires a restart of the devices in order to renumber them into different lanes. Levy states as follows:

> [0042] The DEVICES 0-5 begin their respective port identification methods by clearing their device identifier (ID) in blocks 200, 202, and 204. In one embodiment, the DEVICES 0-5 initiate their port identification methods ***in response to power on reset.*** However, the DEVICES 0-5 in other embodiments may initiate their port identification methods ***in response to other events such as, for example, a root reset or a request to re-identify its ports***. Further, in block 200, DEVICE 0 (the root device) sets its device ID to 0. In one embodiment, the device ID of DEVICE 0 may be hardwired; however, in other embodiments, the device ID of DEVICE 0 may be ***set by the BIOS 108, may be set by reset hardware of the DEVICE 0,*** or may be set by some other mechanisms.

Nowhere in Levy's disclosure of the port identification method does Levy state the devices can be operating, *i.e.* processing or outputting data, while the switch *dynamically* distributes the lanes in response to changes in bandwidth needs. Levy discloses that a root reset will allow the device identifier to change the device ID. Levy does mention that that the devices may initiate their port identification methods in response to other events such as a "request to re-identify its ports." Despite this disclosure, Levy still does not state that this "request to re-identify its ports" may be performed by a "switch ... configured to distribute lanes dynamically during operation to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards." It is respectfully submitted that the Examiner's statement that "lanes are distributed not only during startup or other one-time configuration of machine, but during operation" is wholly unsupported by Levy's disclosure (OA Page 4, 03/24/09). While an Examiner is charged with taking the broadest reasonable interpretation of the claims, an

Examiner may not read features into a reference in order to support an otherwise deficient disclosure. Levy only discloses, "the devices may initiate their port identification methods in response to other events such as a "request to re-identify its ports," and this brief disclosure is insufficient to disclose all the five underlined features above. Levy therefore fails to disclose all the features of Claim 1. The Examiner's reliance on Stufflebeam or Grimaud does not remedy these missing features of Levy. Claim 41 is allowable for similar reasons.

CONCLUSION

In view of the foregoing, Applicants respectfully request that the Examiner consider the elected claims for examination on the merits. Examiner Joni Hsu is cordially invited to contact the undersigned should she have any questions about the above remarks. Timely allowance of the pending claims is requested.

In the event that an appropriate fee amount is not enclosed by check for any fees due in connection with the filing of this Response or requisite extensions of time, please charge any deficiencies or credit any overpayments to Deposit Account No. 50-1349.

Respectfully submitted,

Dated: June 23, 2009

By: Paul Roberts
Celine Jimenez Crowson
Registration No. 40,357

Paul A Roberts
Registration No. 56,990

HOGAN & HARTSON LLP
555 13th Street, N.W.
Washington, D.C. 20004
Telephone: 202-637-5600
Facsimile: 202-637-5910
email: dcptopatent@hhlaw.com
Customer No.: 24633